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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,831	11/04/2003	Kazuhiro Tsuruta	11-202	5569

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EXAMINER	
WARREN, MATTHEW E	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/699,831	TSURUTA, KAZUHIRO	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *6-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/4/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Election filed on January 13, 2005.

Election/Restrictions

Applicant's election without traverse of Group 1, claims 1-5 in the reply filed on January 13, 2005 is acknowledged. Claims 6-25 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuo et al. (US 6,504,227 B1) in view of Rogers et al. (US 4,571,819).

In re claim 1, Matsuo et al. shows (fig. 1) a semiconductor device in which first device components (14) are disposed on an insulating material (13) and second device components are fabricated (15) wherein an oxide layer of 10 μm or more in thickness is formed in a region where the first device components are to be disposed. Matsuo shows all of the elements of the claims except the oxide layer being a thermal-oxide and

a groove packed with a polycrystalline semiconductor is formed at an inward position from the peripheral edge of the thermal-oxide layer and along the same peripheral edge. Rogers et al. shows (fig. 7) a semiconductor device insulating region having a groove with a thermal oxide material (16) and the groove packed with a polycrystalline semiconductor (17) and formed at an inward position from the peripheral edge of the thermal-oxide layer and along the same peripheral edge. The thermal oxide provides stress relief for the substrate and the polysilicon provides etch protection during the planarization process to ultimately preserve the electrical integrity of the device (col. 5, lines 25-41). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the insulating region of Matsuo by using thermal oxide and a polysilicon material in the groove as taught by Rogers to provide stress relieve, etch protection, and preservation of the electrical integrity of the device.

In re claim 2, Rogers discloses (col. 6, lines 44-61) that the groove packed with a polycrystalline semiconductor has a depth larger than the thickness of the oxide layer because the oxide layer may be etched back lower than the polysilicon.

In re claims 4 and 5, Matsuo shows (fig. 1) that said first device components comprise passive components (inductor 14), and said second device components comprise active components (MOSFET 15). The passive components are components that handle high-frequency signals (col. 7, lines 43-59).

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuo et al. (US 6,504,227 B1) in view of Rogers et al. (US 4,571,819) as applied to claim 1 above, and further in view of Geissler et al. (US 6,245,600 B1).

In re claim 3, Matsuo and Rogers show all of the elements of the claims except semiconductor substrate comprises a silicon-on-insulator substrate, and said thermal-oxide layer reaches a buried oxide film layer of the silicon-on-insulator substrate. Geissler et al. discloses (col. 1, lines 13-22) that is well known that bulk semiconductor devices can be formed on SOI substrates for higher performance, latch-up absence, high packing density, and low voltage applications. When combined with Matsuo and Rogers, the thermal-oxide layer may reach the buried oxide layer of the SOI depending on the thickness of the silicon on the insulator and the depth of the thermal oxide. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the bulk device of Matsuo and Rogers by forming the device on an SOI substrate as taught by Geissler for higher performance, latch-up absence, high packing density, and low voltage applications.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Boyd et al. (US 5,726,084) and Hatanaka (US 6,566,226 B2) also show insulation regions formed in a substrate and having polysilicon semiconductor materials about the peripheral edge of the oxide in the regions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW

April 29, 2005

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER